## REMARKS/ARGUMENTS

Claims 1-23 are pending in the present application. Claims 1-7, 9-15 and 17-23 are amended. Reconsideration of the claims is respectfully requested.

### I. Interview Summary

Applicants thank the Examiner for the interview held on November 28, 2006 between the Applicant's representative and the Examiner. The rejection of claim 1 under 35 U.S.C. § 102(e) was discussed. No agreement was reached.

### II. Amendments to the Claims

Claims 1-7, 9-15 and 17-23 are amended. Support for the claim amendments can be found in the Applicant's patent application on page 7, lines 13-23; page 8, lines 17-29; page 9, line 16 through page 10, line 16; and page 11, line 21 through page 12, line 20. The claims should now be in allowable form.

### III. 35 U.S.C. § 102, Anticipation

The Office Action rejected amended claims 1-4, 7, 9-12, 15, 17-20 and 23 under 35 U.S.C. § 102(e) as anticipated by *Kumar*, Method and Apparatus for Setting Timing Parameters, U.S. Patent No. 7,096,377 (March 27, 2002) (hereinafter "*Kumar*"). This rejection is respectfully traversed.

With respect to amended claim 1, the Office Action states:

> As per claim 1, Kumar teaches a method in a multi-processor data processing system for changing an operating frequency for a system core logic used to interface to memory in the data processing system, the method comprising:
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> determining whether the operating frequency should be changed from a default frequency to another frequency (col. 1, lines 46-57, ". . . choose common clock speed that will enable all the components to work together"; col. 5, line 65 – col. 6, line 17, ". . . calculate a parameter value . . . that would enable the processors, logic 320 and/or memory 330 to work together", where system core logic normally runs at default frequency – e.g. see Applicant's admitted prior art p. 2, lines 2-14);
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> responsive to determining the operating frequency should be changed from the default frequency to the another frequency, placing slave processors in the multi-processor data processing system into a non-transactional mode (col. 3, lines 1-34, in response to querying that occurs before placing processor in non-transactional mode; col. 4, lines 35-47; col. 5, lines 4-21, some processors are inherently designated as slave processors); and
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> changing the operating frequency in the system core logic to the another frequency (col. 5, line 65 – col. 6, line 17, ". . . set . . . logic 320 with the calculated parameters. . .").

Office Action dated September 18, 2006, pages 2-3.

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, every feature of the presently claimed invention is not identically shown in *Kumar*, arranged as they are recited in the claims.

Amended claim 1 is representative of amended claims 9, 17 and 23. *Kumar* does not anticipate amended claim 1 because *Kumar* does not disclose each and every feature of amended claim 1. Amended claim 1 is as follows:

> 1. A method in a multi-processor data processing system, having at least one master processor, at least one slave processor, memory, and a system core logic used to interface the processors to the memory, for changing an operating frequency of the system core logic, the method comprising:
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> determining whether the operating frequency of the system core logic should be changed from a first frequency to a second frequency;
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> responsive to determining the operating frequency should be changed, placing the at least one slave processor into a non-transactional mode; and
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> responsive to placing the at least one slave processor into the non-transactional mode, changing the operating frequency of the system core logic to the second frequency.

*Kumar* does not disclose all the features of amended claim 1. Specifically, *Kumar* fails to disclose (1) the feature of responsive to determining the operating frequency should be changed, placing the at least one slave processor into a non-transactional mode, and (2) the feature of determining whether the operating frequency of the system core logic should be changed from a first frequency to a second frequency.

First, *Kumar* fails to disclose the feature of responsive to determining the operating frequency should be changed, placing the at least one slave processor into a non-transactional mode. The Office Action asserts that *Kumar* discloses the feature of placing slave processors into a non-transactional mode, as recited in amended claim 1. Specifically, the Office Action refers to column 3, lines 1 through 34, column 4, lines 35 though 47, and column 5, lines 4 though 21 of *Kumar*. The cited references are as follows:

> [Column 3, lines 1-21] At a predetermined time, such as when computer system 100 is powered on, reset and/or initialized, system management controller 180 controls logic 120 via bus 184, causing logic 120 to hold the processor installed at processor socket 110 via bus 115 in a reset or other state such that the processor does not perform transactions on bus 115. The holding of the processor in such a state by way of logic 120 could be accomplished by causing logic 120

to signal the processor using one or more control lines provided by bus 115. Alternatively, the processor may execute a series of instructions that causes it to wait or halt, or to in some other way coordinate with system management controller 180 at the predetermined time such that the processor refrains from engaging in transactions on bus 115. As an alternative to using logic 120, system management controller 180 might directly control the processor installed at processor socket 110 via bus 182 to prevent the processor from performing transactions on bus 115. Again, this could be accomplished using a control line provided by bus 182, or by the processor executing code causing the processor to coordinate with system management controller 180.

[Column 3, lines 22-34] Either while the processor is being held in such a state or at an earlier time, system management controller 180 uses bus 182 to query the processor for minimum and/or maximum limits regarding one or more timing parameters for the processor's interface to bus 115 and/or for one or more internal timing parameters of the processor, itself. System management controller 180 may also use bus 184 to query logic 120 for similar parameters regarding logic 120 or its interface to bus 115. System management controller 180 uses one or more of these parameters to calculate a parameter value at which bus 115, the processor and/or logic 120 could be set that would enable the processor and logic 120 to work together through bus 115.

[Column 4, lines 35-47] Although computer system 200 is depicted as having sockets for two processors, computer system 200 may be implemented with three, four or more processors, and these processors may all share a single bus, such as bus 215, or may be distributed among multiple busses. In support of larger numbers of processors, the functions performed by logic 220 may be distributed, and perhaps duplicated, among multiple incarnations of logic 220, especially if the multiple processors are distributed among multiple busses. Furthermore, regardless of the number of processors and/or incarnations of logic 220, computer system 200 may be comprised of multiple incarnations of I/O bus bridge 240.

[Column 5, lines 4-21] Using one of the techniques discussed above with regard to computer system 100 of FIG. 1, at a predetermined time, system management controller 280 causes the processors installed at processor sockets 210 and 212 to refrain from performing transactions on bus 215. System management controller 280 uses bus 282 to query the processors for one or more parameters of the variety previously discussed with regard to computer system 100 of FIG. 1. System management controller 280 may also similarly use bus 284 to query logic 220 for one or more of such parameters for logic 220. System management controller 280 uses one or more of these parameters to calculate a parameter value at which bus 215, the processors and/or the logic 220 could be set that would enable the processors and logic 220 to work together through bus 215. System management controller 280 would then set either the processor or logic 220 with the calculated parameters using one of the techniques previously discussed with regard to computer system 100 of FIG. 1.

*Kumar*, column 3, lines 1-34 column 4, lines 35-47 and column 5, lines 4 though 21.

Neither the cited sections of *Kumar*, nor any other section of *Kumar* discloses the feature of placing the at least one slave processor into a non-transactional mode as recited in amended claim 1 of the presently claimed invention, because *Kumar* fails to distinguish between processors when placing them in non-transactional mode. The cited sections of *Kumar* disclose the process of halting system processors, thereby allowing the system management controller to calculate parameters for the internal operation of the computer system, such as internal timing parameters. The cited sections of *Kumar* then disclose the same process in the multi-processor context, whereby multiple processors are halted so that system parameters may be calculated by the system management controller. However, the system processors as well as multi-processors in *Kumar* are not the same as a slave processor, as recited in amended claim 1.

On the other hand, amended claim 1 recites the feature of at least one slave processor. Nowhere in the cited text or elsewhere in *Kumar* does *Kumar* mention a slave processor, let alone distinguish between the system processors or the multi-processors and other processors. In the Examiner interview, the Examiner stated that the system processors are slave processors because the system management controller is the master processor. However, the Examiner misapprehends the cited text.

*Kumar*, when describing a multi-processor computer system, refers to all of the processors in the computer system as a single unit and does not specifically distinguish between the system processor and the processor within the system management controller. Therefore, *Kumar* does not disclose slave processors. Furthermore, even if *Kumar* does distinguish between the processors, *Kumar* never intended to distinguish between the system processor and the processor within the system management controller. *Kumar* always refers to the functions of the processors as single unit. For example, *Kumar* discloses a computer system that "causes the processors installed at processor sockets 210 and 212 to refrain from performing transactions on bus 215," wherein the processors installed at processor sockets 210 and 212 constitute all of the processors located in the computer system. *See e.g.* column 5, lines 4-8. More specifically, when referring to the halting process, *Kumar* also only discloses the processors performing the halting process as a single unit. Even though *Kumar* discloses that processors may at least partially carry out the functions of the system management controller, the partial functions carried out by the system processors still fail to distinguish between processors in the computer system when disclosing placing processors to a non-transaction mode, as recited in amended claim 1. Therefore, *Kumar* does not distinguish between processors within the computer system, much less designate less than all of the processors in the computer system as slave processors. Thus, *Kumar* does not anticipate the feature of placing the at least one slave processor into a non-transactional mode.

Additionally, *Kumar* does not inherently designate any processor as a slave processor. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. MPEP 2112. To establish inherency, the extrinsic evidence

must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, may not be established by probabilities or possibilities. The fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency. MPEP 2112 and *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Furthermore, in relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. MPEP 2112 and *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

In this case, the Office Action has not proven that slave processors are necessarily designated in *Kumar*. Additionally, *Kumar* cannot show that some processors are designated as slave processors because *Kumar* does not distinguish between processors at all. Absent some distinction between processors, *Kumar* does establish the possibility of designating some of the processors as slave processors, much less establish that slave processors are necessary. Moreover, a plausible alternative exists in that *Kumar's* process will work as intended when no processors are slave processors. Therefore, the existence of slave processors is not *necessarily* present in *Kumar*. For this reason, *Kumar* does not inherently teach any processor as being a slave processor, as claimed. As shown above, *Kumar* does not explicitly teach this claimed feature. Accordingly, *Kumar* does not anticipate amended claim 1.

Second, *Kumar* also does not disclose the feature of determining whether the operating frequency of the system core logic should be changed from a first frequency to a second frequency, as recited in amended claim 1. The Office Action asserts otherwise, specifically citing to column 1, lines 46 through 57 and column 5, line 65 through column 6, line 17 of *Kumar*. The Office Action also cites to page 2, lines 2 through 14 of Applicant's patent application. The cited sections are as follows:

> [*Kumar*, column 1, lines 46-57] Difficulties arise when two components are connected by such an interface where one of the two components is able to function with that interface having a higher clock speed than the other component. It is commonly left to those who assemble such components together to determine the minimum and maximum clock speeds at which the interface of each component can be operated, and to choose a common clock speed that will enable all of the components to work together. It is also commonly left to those who assemble such components together to determine the minimum and maximum clock speed of the internal clock of at least one of the components, and to choose a ratio between the common clock speed chosen for interface and the internal clock speed of that component.
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> [*Kumar*, column 5, line 65 – column 6, line 17] Using one of the techniques discussed above with regard to computer system 100 of FIG. 1, at a predetermined time, system management controller 380 causes the processor installed at processor socket 310 to refrain from performing transactions on bus 315. System management controller 380 may use bus 382 to query the processor attached to socket 310 for one or more parameters of the variety previously

> discussed with regard to computer system 100 of FIG. 1. System management controller 380 may also similarly use busses 384 or 386 to query logic 320 or memory 330, respectively, for one or more similar parameters. System management controller 380 uses one or more of these parameters to calculate a parameter value at which bus 315, bus 335, the processor, logic 320 and/or memory 330 could be set that would enable the processors, logic 320 and/or memory 330 to work together. System management controller 380 would then set either the processor or logic 320 with the calculated parameters as previously discussed with regard to computer system 100 of FIG. 1.
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> [Applicant's Patent Application, page 2, lines 2-14] A data processing system may contain DIMMs running at two different memory speeds, such as 333mHz and 400mHz. The system core logic, also referred to as an I/O bridge, generates a clock signal used to drive data on the bus in the data processing system. This system core logic normally runs at a default base frequency to allow the system firmware to initialize the memory and other I/O subsystems. When a data processing system has only high speed DIMMs, it is desirable to move the core operating frequency of the system core logic to that of the high speed DIMMs to increase the bandwidth of the system memory. The operating frequency is often set through a basic input/output system (BIOS).

*Kumar*, column 1, lines 46-57, column 5, line 65 – column 6, line 17; Applicant's patent application, page 2, lines 2 through 14.

Neither the cited sections, nor any other section of *Kumar* discloses the claimed feature, because *Kumar* only discloses choosing a single frequency that allows system components to work together. *Kumar* does not teach a determination of whether the operating frequency should be changed. The cited sections of *Kumar* present the problem of coordinating system components that operate on different frequencies. *Kumar* discloses that the selection of a parameter, such as a frequency, enables components within a computer system to "work together." See *Kumar*, column 1, lines 51-52 and column 6, line 13.

The Office Action also cites page 2 of the Applicant's patent application, which discloses the existence of a multi-processor system that runs at a default frequency at initialization. However, the choosing of a single parameter, like a frequency, is not the same as determining whether an operating frequency should be changed.

On the other hand, amended claim 1 recites determining whether the operating frequency of the system core logic should be changed from a first frequency to a second frequency. The disclosure of *Kumar* differs from the claimed feature of amended claim 1, because the claimed feature determines whether the operating frequency should be changed, while *Kumar* discloses only the selection of a single frequency that allows system components to work together. In other words, *Kumar* teaches the selection of a frequency that allows system components to work together, while the claimed feature determines whether a change in operating frequency should occur. Therefore, *Kumar* does not disclose all the features of amended claim 1.

In addition, *Kumar* does not disclose the feature of responsive to determining the operating frequency should be changed, placing the at least one slave processor into a non-transactional mode, as recited in amended claim 1. The Office Action asserts otherwise, citing specifically to column 3, lines 1 through 34, column 4, lines 35 though 47, and column 5, lines 4 though 21 of *Kumar*. The cited sections are presented above.

However, *Kumar* fails to anticipate the claimed feature, because *Kumar* only discloses putting processors in a non-transactional state at a "predetermined time" and not in response to a determination. The cited sections of *Kumar* describe the process of halting system processors at a pre-determined time so that a frequency may be chosen for the system. The only clues given as to the meaning of "predetermined time" occur at column 3, lines 1-3, wherein the system is powered-on, reset, or initialized. However, a "predetermined time" is not the same as recited in amended claim 1, because a predetermined time is not in response to a determination.

On the other hand, amended claim 1 recites the feature of responsive to determining the operating frequency should be changed, placing the at least one slave processor into a non-transactional mode. Amended claim 1 links the determination of changing the operating frequency with placing at least one slave processor into a non-transactional mode. In other words, the feature of placing is in response to the determination. As shown above, *Kumar* fails to disclose either the features of determining the desirability of a frequency change or placing a slave processor into non-transactional mode. *Kumar* therefore does not disclose any relationship between the two features, much less a "response to" relationship between the two features. Therefore, *Kumar* does not disclose the feature of responsive to determining the operating frequency should be changed, placing the at least one slave processor into a non-transactional mode. Therefore, *Kumar* does not disclose all the features of amended claim 1. Accordingly, *Kumar* does not anticipate amended claim 1.

Because amended claim 1 is representative of amended claims 9, 17 and 23, the same distinctions between amended claim 1 and the references also apply to amended claims 9, 17 and 23. Additionally, because amended claims 2-4, 7, 10-12, 15 and 18-20 depend from amended claims 1, 9, and 17, the same distinctions between *Kumar* and the inventions of amended claims 1, 9 and 17 apply for these amended claims as well. Accordingly, the rejection of amended claims 1-4, 7, 9-12, 15, 17-20 and 23 under 35 U.S.C. § 102(e) has been overcome.

## IV. 35 U.S.C. § 103, Obviousness: Claims 5, 13 and 21

The Office Action rejected amended claims 5, 13 and 21 under 35 U.S.C. § 103(a) as obvious over *Kumar* as applied to amended claims 1, 9 and 17 above in view of *Lee*, Method and Apparatus for Implementing a Stop State for a Processor in a Multiprocessor System, U.S. Patent No. 5,867,658 (April 4, 1997) (hereinafter "*Lee*"). This rejection is respectfully traversed.

With regard to amended claims 5, 13 and 21, the Office Action states:

> As per claims 5, 13 and 21, Kumar teaches the non-transactional mode is one of various possible modes in which the slave processors do not generating any external bus transactions (col. 3, lines 1-21; col. 5, lines 6-21), but does not expressly teach the non-transactional mode as being a spin loop. Lee teaches that being in a spin loop is one known form of non-transactional mode (col. 2, lines 52-67). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Lee's executing spin loop as Kumar's non-transactional mode, as executing a spin loop is a known alternative for halting a processor.

Office Action dated September 18, 2006, page 6.

A *prima facie* obviousness rejection cannot be made against amended claim 5 because neither reference, alone or in combination, teaches or suggests all the features of amended claim 5. The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Additionally, all limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). In the case at hand, the proposed combination does not teach all of the features of the claimed invention.

Amended claim 5 is representative of amended claims 13 and 21. Amended claim 5 is as follows:

> 5. The method of claim 1, wherein the non-transactional mode comprises one of a sleep mode or a mode in which the slave processor is in a spin loop without generating any external bus transactions to the system core logic.

A *prima facie* obviousness rejection cannot be made because the proposed combination of the references does not teach all of the features of amended claim 5. As shown above, *Kumar* does not disclose all the features of amended claim 1. Therefore, *Kumar* also does not disclose all the features of amended claim 5, which depends from amended claim 1.

*Lee* does not cure *Kumar's* lack of disclosure regarding claim 1. *Lee* discloses a method for implementing a stop state for a processor and the communication and storage of signature data to determine a processor's status. *Lee* discloses that a processor may be prevented from executing instructions by placing the processor in a spin loop. *Lee* fails to disclose or suggest any of the features of amended claim 1.

As established above, neither *Kumar* nor *Lee* teach or suggest all of the features of amended claim 1. Therefore, the proposed combination of *Kumar* and *Lee*, when considered as a whole, does not teach all of the features of amended claim 5, which depends from amended claim 1. Accordingly, the Office Action has failed to state a *prima facie* obviousness rejection against amended claim 5.

Furthermore, the Office Action fails to establish a *prima facie* case of obviousness, because the Office Action fails to provide a proper teaching, suggestion, or motivation to combine the references. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. The teaching or suggestion to make the claimed combination must be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP 2143.01.

In the case at hand, a *prima facie* obviousness rejection cannot be made because a proper motivation to combine the references does not exist. The Office Action does state that "[a]t the time of the invention, it would have been obvious to one of ordinary skill in the art to apply *Lee*'s executing spin loop as *Kumar*'s non-transactional mode, as executing a spin loop is a known alternative for halting a processor." Office Action, page 6. However, this statement, in it of itself, does not state a teaching, suggestion, or motivation to combine the references to achieve the invention as recited in original claim 5. Specifically, the statement identifies no teaching, suggestion or motivation to combine the spin loop disclosed in *Lee* with the apparatus for setting timing parameters disclosed in *Kumar* to achieve the invention of original claim 5. Additionally, no motivation exists to add the claimed features not disclosed in the cited references to the proposed combination. Therefore, the statement also cannot serve as a proper teaching, suggestion, or motivation to combine the references and no such teaching, suggestion, or motivation exists. Accordingly, no *prima facie* case of obviousness can be made against amended claim 5.

Because amended claim 5 is representative of amended claims 13 and 21, the same distinctions between amended claim 5 and the references also apply to amended claims 13 and 21. Accordingly, the rejection of amended claims 5, 13 and 21 under 35 U.S.C. § 103(a) has been overcome.

## V. 35 U.S.C. § 103, Obviousness: Claims 6, 8, 14, 16 and 22

The Office Action rejected amended claim 6, claim 8, amended claim 14, claim 16 and amended claim 22 under 35 U.S.C. § 103(a) as obvious over *Kumar* as applied to amended claims 1, 9 and 17 above, and further in view of *Kurosawa*, Integrated Circuit Device Having Clock Frequency Changing Function, Computer System Using the Integrated Circuit Device and Clock Frequency Changing Method, U.S. Patent No. 6,643,792 (September 20, 2000) (hereinafter "*Kurosawa*"). This rejection is respectfully traversed.

With regard to amended claim 6, claim 8, amended claim 14, claim 16 and amended claim 22, the Office Action states:

> As per claims 6, 14 and 22, Kumar does not expressly teach the changing step comprises setting a register in the system core logic to a value for the another frequency. Kurowasa [sic] teaches such details for a changing step (fig. 1, setting register R of clock generator within host PCI-bridge 6; col. 9, lines 4-21). At the time of the invention, it would have been obvious to one of ordinary skill in the art that Kurowasa's [sic] register setting is applicable to Kumar's method, as such register setting is a common method for changing the operating frequency of system core logic.
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> As per claims 8 and 16, symmetric multiprocessing (SMP), in which identical processors share system memory, is well-known in the art.

Office Action dated September 18, 2006, page 6.

No *prima facie* obviousness rejection can be made against amended claim 6 or claim 8 because the proposed combination of the references does not teach or suggest all of the features of amended claim 6 or claim 8. Amended claim 6 is representative of amended claims 14 and 22. Amended claim 6 is as follows:

> 6. The method of claim 1, wherein the changing step comprises:
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> setting a register in the system core logic to a value of the second frequency;
>
> entering, by the master processor, a delay loop to prevent sending transactions to the system core logic; and
>
> in response to termination of the delay loop, checking, by the master processor, the register in the system core logic to ensure the operating frequency of system core logic has been changed to the second frequency.

Claim 8 is representative of claim 16. Claim 8 is as follows:

> 8. The method of claim 1, wherein the multi-processor data processing system is a symmetric multi-processor data processing system.

No *prima facie* obviousness rejection can be made because the proposed combination of the references does not teach all of the features of amended claim 6 or claim 8. As shown above, *Kumar* does

not disclose all the features of amended claim 1. Therefore, *Kumar* also does not disclose all the features of amended claim 6 or claim 8, which depend on amended claim 1

*Kurosawa* does not cure *Kumar*'s lack of disclosure. *Kurosawa* discloses a computer system in which the clock frequency may be changed to synchronize multiple large-scale integrated circuits using signals indicating clock frequency status. Although *Kurosawa* does disclose setting a register to designate a frequency to which the computer system may be set, the setting of a register is still not the same as the features distinguished in amended claim 1. *Kurosawa* fails to disclose any of the features of amended claim 1. Therefore, the proposed combination of *Kumar* and *Kurosawa* does not teach all of the features of amended claim 6 or claim 8. Accordingly, the Office Action fails to state a *prima facie* obviousness rejection against amended claim 6 or claim 8.

Additionally, no *prima facie* obviousness rejection can be made because no proper teaching, suggestion, or motivation to combine the references exists. The Office Action does state that "[a]t the time of the invention, it would have been obvious to one of ordinary skill in the art that Kurowasa's [sic] register setting is applicable to *Kumar*'s method, as such register setting is a common method for changing the operating frequency of system core logic." However, this statement does not state a teaching, suggestion, or motivation to combine the references to achieve the invention of amended claim 6. Specifically, the statement identifies no teaching, suggestion or motivation to combine the register setting disclosed in *Kurosawa* with the apparatus for setting timing parameters disclosed in *Kumar* to achieve the invention of amended claim 6. Therefore, this statement cannot be used to provide a proper motivation to combine the references in the manner suggested by the Examiner or in a manner to render obvious amended claim 6. Accordingly, no *prima facie* case of obviousness can be made against amended claim 6.

With regard to claim 8, the Office Action states that "symmetric multiprocessing (SMP), in which identical processors share system memory, is well-known in the art." For the same reasons presented above in regard to amended claim 6, this statement cannot provide a proper teaching, suggestion, or motivation to combine the references to achieve the invention of claim 8. Accordingly, no *prima facie* case of obviousness can be stated against claim 8.

Because amended claim 6 is representative amended claims 14 and 22, the same distinctions between amended claim 6 and the references also apply to amended claims 14 and 22. Because claim 8 is representative of claim 16, the same distinctions between claim 8 and the references also apply to claim 16. Accordingly, the rejection of amended claim 6, claim 8, amended claim 14, claim 16 and amended claim 22 under 35 U.S.C. § 103(a) has been overcome.

## VI. Conclusion

It is respectfully urged that the subject application is patentable over *Kumar*, *Kumar* in view of *Lee*, and *Kumar* in view of *Kurosawa* and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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